Addressing the DC offset challenge in direct conversion RF receivers

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Introduction

Direct conversion radio techniques have been widely adopted in recent years for cellular and other wireless communications applications, where they have both simplified design and lowered component costs compared with conventional superheterodyne receiver designs. However there are also drawbacks in taking this approach, of which the principal one is the DC offset voltages that occur within the down-converter mixer stage. This white paper explores the use of direct conversion for RF applications such as private mobile radio (PMR) or satellite communications, including an investigation into some of the causes of DC offsets and an outline of some steps that can be taken to minimise them.

Superheterodyne, zero IF and low IF

The classic superheterodyne receiver uses two (or more) stages of down-conversion, firstly from RF to an intermediate frequency (IF), and then from IF to baseband. Typically two local oscillators (LO) are used to mix with the received signal and then IF signal. This technique has the advantages including that channel filtering is simpler at the IF. However it can cause problems, principally due to the production of image and spurious responses caused by additional mixing products of the RF and LO in addition to the signal at the difference frequency (IF).

When direct conversion (also referred to as zero IF) is employed, the LO is at the same frequency as the wanted RF signal, and the signal is down-converted directly to baseband. This removes the need for the bandpass filters that are normally used in a superheterodyne design to remove the image frequencies, and results in a more compact device with a lower bill of materials. Mixing the signal down to 0 Hz (zero IF) by setting mixer LO and frequencies to be the same value avoids placing the image of the adjacent channel and other close-in interferers into the same frequency band as the wanted modulation. This is of particular benefit in cases where large adjacent channel interferers occur. The zero IF approach also minimises the bandwidth of I/Q output signals, which reduces the cost, power and complexity of the analogue-to-digital converters (ADCs) used to sample them. Lastly, it enables a low-pass filter to be used on each of I and Q signal paths to provide selectivity. This simplifies design by reducing filter complexity and the required dynamic range of the ADCs.

Two alternative approaches are near-zero IF (NZIF), where the LO is offset from the carrier by a small frequency difference, and low IF, where this difference is slightly higher but still much lower than in a superheterodyne system. Near-zero IF I/Q architectures typically set the LO frequency to a multiple of 0.25 to 1 with respect to the required channel bandwidth, which provides frequency separation between the wanted signal and any DC components in the output I and Q signals. These receivers then sample (ADC convert) the near-zero I/Q IF signal pair, and then use digital baseband processing both to implement a simple high-pass filter to remove the DC component and to perform a final frequency mix down to 0 Hz. Operating in a near-zero IF mode requires the baseband low-pass filters to have a wider bandwidth to pass the chosen IF frequency, and also requires the sampling ADC bandwidth to be broader, and therefore higher in power, than ADCs used in the zero IF architecture. Another, and perhaps more significant, trade-off of near-zero IF is that the adjacent channel image generated by unavoidable I/Q gain and phase errors typically now coincides with the wanted signal, creating a significant interference component if the adjacent channel signal level is high.

In a low-IF I/Q architecture, the mixer LO frequency is set to have a larger frequency separation from the wanted RF carrier frequency than in the near-zero IF case. This means that the wanted signal is mixed to an even higher frequency at the I/Q outputs, enabling receiver I/Q outputs to potentially be AC coupled to ADCs. Low IF I/Q trade-offs are similar to those relating to near-zero IF, but are more challenging in that ADCs with a wider bandwidth must be used and the image rejection issue is worse.

Direct conversion architecture

Figure 1 shows a typical RF front end, based on the CMX994A direct conversion receiver, which operates up to around 1 GHz. The chip has a broadband low-noise amplifier (LNA) with gain control at the input, followed by a high dynamic range I/Q demodulator with a very high second-order intercept point (IIP2). In this example LO generation is either provided by an internal integer-N PLL and negative resistance VCO, or alternatively can be input from an external LO. The receiver baseband section requires further amplification, and also baseband filter stages that have precise, configurable bandwidth. Flexible multi-band operation is enabled by the use of LO dividers.

There are a few applications where an off-chip LNA has some benefits, for example in designs where a 50Ω match is required across a very broad operating band, or in those where absolute maximum sensitivity is required – and where intermodulation rejection is less important – as in some satellite communication systems. LNA gain control before the I/Q mixers is important in the case of high input signal levels, as it minimises issues with second order intermodulation (IP2) products and local oscillator pulling. For this reason if an external LNA is used then gain control should be included.

A key objective of the CMX994 family ICs is to meet the demanding receiver requirements in Europe under the Radio Equipment Directive such as EN 300 113 for digital PMR and narrowband wireless data systems.

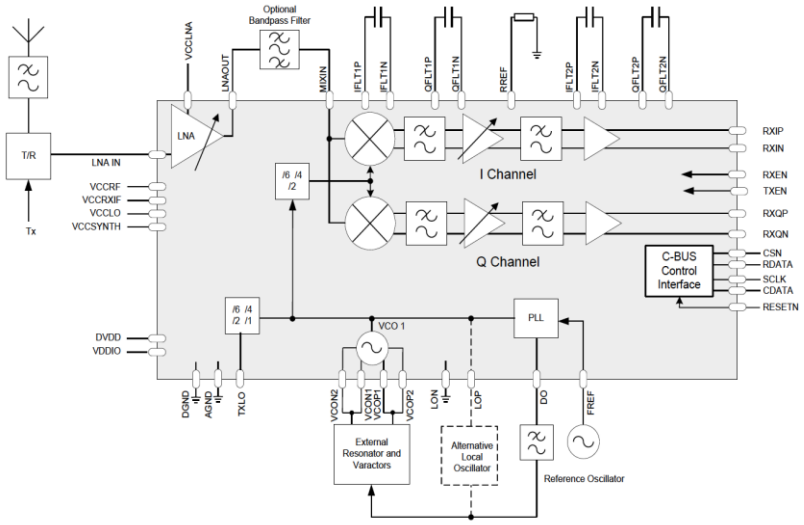

Figure 1: Architecture of direct conversion receiver with either on-chip or off-chip local oscillator

Causes of DC offset

Inevitably some leakage occurs between the LO and RF input path to the mixer – particularly coupling to the LNA input, which will amplify the leakage – this leakage signal will produce an unwanted DC component when it mixes with the LO (self-mixing). A large DC signal will reduce the dynamic range available in the system. AC coupling can be used to mitigate the DC offset effects but is generally avoided because it can have a detrimental effect because the AC capacitor influences the low frequency content of the baseband signal, which can seriously affect the subsequent decoding algorithm. A simple illustration of DC offset is shown in figure 2.

The other notable cause of DC offsets is the presence of a strong in-band interference source(s) in the received signal. AM modulated signals are particularly problematic with the receiver second order intermodulation (IM2) response producing varying DC. Near-zero IF and low IF systems are not as susceptible to IM2 DC offsets as true zero IF (direct conversion) designs.

DC offsets vary somewhat with receive channel, LO level and, to some extent, with time and temperature. In order to achieve the best receiver dynamic range, it is necessary to estimate DC offsets to a high degree of precision, typically 70–80 dB below the ADC full-scale. In principle it is possible to measure the DC offset by averaging the receiver noise without the presence of a signal. If averaging is attempted with a signal present, the DC offset result can be influenced by an unbalanced data pattern in the modulation: in this case it can be helpful to know the characteristics of the signal, in order to optimise the DC offset algorithm. Furthermore, if there is gain between the receiver output and the ADC – particularly if that gain is adjusted as part of an AGC mechanism – the effect of the gain on DC offsets must be considered.

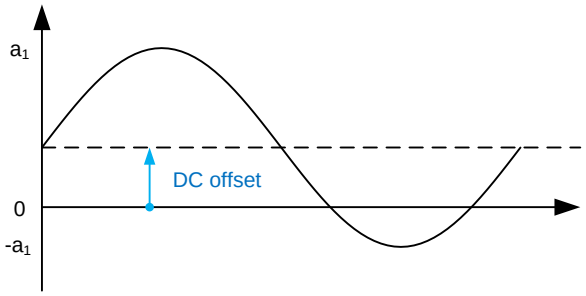

Figure 2: Illustration of DC offset on a sine wave signal

DC offset mitigation

For true direct conversion receivers, minimising the challenge of DC offsets requires careful design of the receiver demodulator. Initially the problem can be minimised by ensuring that the mixer that is used has extremely good IIP2 performance, because – like the down-converted signal – second order mixer intermodulation products occur at 0Hz (DC). The CMX994/CMX994A/CMX994E receivers are specified with typically +79 dBm mixer IIP2 performance in order to attenuate such DC intermodulation products.

An approximate correction of DC offsets that do occur can be made over the serial interface using the Rx Offset Register (0x13). This is performed using small voltages injected at the mixer outputs (Figure 4).

The setup procedure is as follows: with the gain control set at maximum, the offset at the I or Q output is measured, then the figures in Table 1 are used to give the appropriate bit settings for the required offset correction for both the I and Q paths. The range double bit — register 0x12, bit 2 – can also be used to increase the correction range if required. The bits in registers 0x13 and 0x17 control the same hardware functions, with the most recent write to either register being applied at any given time.

The values in Table 1 reflect the effects of the offset at the maximum VGA gain (minimum attenuation) setting. They are proportionally lower for lower gain settings. The aim of this Rx Offset Register is to allow output offsets to be reduced sufficiently (typically to less than 25 mV) to avoid any significant reduction in the dynamic range of any subsequent ADC. Applying the correction close to the start of the I/Q baseband chain maximises the dynamic range in the analogue sections. The remaining offset needs to be corrected using the demodulation software in the baseband processor, as part of the demodulation process.

It should be noted that at high attenuation settings there may be an additional error due to residual offsets from within the VGA.

Bit number b3 b7	Bit number b2 b6	Bit number b1 b5	Bit number b0 b4	Correction in mV I channel at maximum gain Q channel at maximum gain
1	1	1	1	-175
1	1	1	0	-150
1	1	0	1	-125
1	1	0	0	-100
1	0	1	1	-75
1	0	1	0	-50
1	0	0	1	-25
1	0	0	0	0
0	1	1	1	+175
0	1	1	0	+150
0	1	0	1	+125
0	1	0	0	+100
0	0	1	1	+75
0	0	1	0	+50
0	0	0	1	+25
0	0	0	0	0

Table 1

The DC offsets in the CMX994 baseband path are shown in Figure 3. Although the voltages are only shown for the Q path, the same principle also applies to the I path. The DC offsets in I and Q paths may not be the same because offsets in a number of components contribute to the total figure.

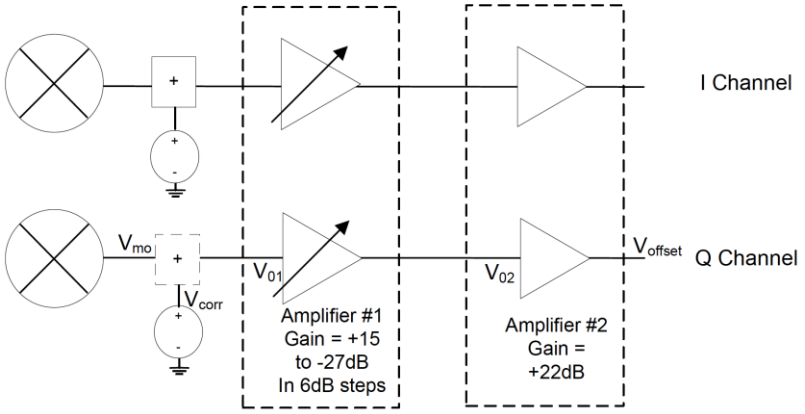

Figure 3: Applying correction voltages to I and Q channels

As mentioned above, the digitally controlled DC offset correction is capable of reducing the offset to 25 mV or less for errors of up to ±200 mV for CMX994, or for errors up to ±800 mV for CMX994A/CMX994E. This represents a reduction in dynamic range of about 0.1 dB for a typical ADC input signal range of 2 V peak–peak and is therefore negligible.

Because the correction in the I and Q paths is applied in a differential manner, both positive and negative corrections are possible, allowing the DC to be normalised to the nominal DC bias level. The voltage sources are scaled in a binary fashion, as shown in Figure 4 for the CMX994, so that multiple sources can be added to provide the desired correction. The same arrangement applies independently on both I and Q channels. Table 2 shows the corrections applied by each of these sources in the CMX994 scheme. For the CMX994A/CMX994E, four additional sources can be used to increase correction range.

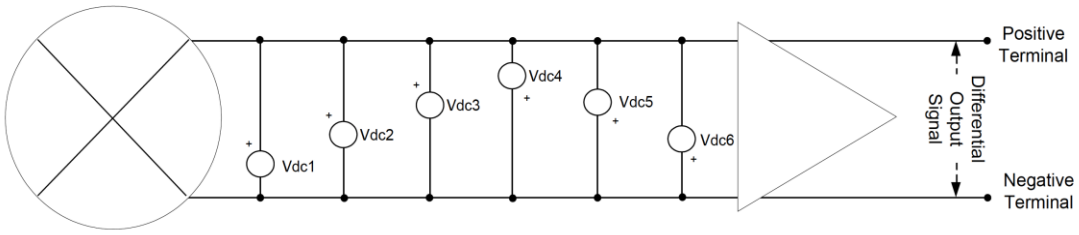

Figure 4: Simplified schematic of the application of DC offset corrections

Source	Voltage correction at output for maximum gain in baseband amplifiers	Correction Polarity
VDC1	25mV	Positive terminal increase, negative terminal decrease
VDC2	50mV	Positive terminal increase, negative terminal decrease
VDC3	100mV	Positive terminal increase, negative terminal decrease
VDC4	25mV	Positive terminal increase, negative terminal decrease
VDC5	50mV	Positive terminal increase, negative terminal decrease
VDC6	100mV	Positive terminal increase, negative terminal decrease

Table 2: DC offset correction adjustments

Fine offset correction

After the coarse correction has been made, a fine DC offset correction can be performed, during which the modem attempts to find the best DC offset in the absence of a signal. This can be achieved by turning off the LNA to reduce the likelihood of signals being present during the DC offset measurement, although if very large signals are present on the channel then they may still disturb the DC measurement. When signals are present it is necessary to manage the DC offset algorithm in order to prevent DC tracking caused by unbalanced modulation – one solution is to have multiple time constants such as 'fast track', 'slow track' and 'hold'.

When the receiver is dealing with strong signals, the accuracy of the DC offset correction becomes less important because the signal level is large compared to the potential offset. This is particularly true with digital systems, where the bit error rate (BER) can be reduced until reception is essentially error-free and further optimisation is not required. Care should be taken to ensure that DC offset estimates measured with large signals are still valid at lower signal levels, particularly if receiver gain has been adjusted by the AGC system. It is therefore beneficial for the AGC and DC offset systems to be designed to complement each other, such as by having DC offsets adjusted to values that have been stored for each gain step.

Baseband processor

A direct receiver such as the CMX994/CMX994A/CMX994E requires the use of a device such as the CMX983 Analogue Front End, which provides the interface between the RF section of the digital radio and the DSP/FPGA. This front end, designed to meet the needs of a software-defined radio (SDR), provides dual-channel analogue-to-digital and digital-to-analogue conversion, integrating several auxiliary ADCs and DACs for use within the radio system and also including two RF fractional-N synthesisers, to provide a complete small form factor, RF-to-digitised baseband solution.

This approach is compatible with the SDR model, where a common hardware platform can be used across a number of radio systems. System-specific operation and functions are fully software-based within the DSP/microcontroller, where further corrections for errors cause by DC offsets can be compensated for.

Alternatively CML offers modem ICs such as the CMX7341 and CMX7164 that provide full DC offset mitigation with automatic control of the CMX994/CMX994A/CMX994E. Modulations supported are diverse as 64-QAM, 4-FSK, GMSK and analogue FM.

Conclusion

Direct conversion presents the ideal solution for a high performance yet low-cost radio system, provided that DC offsets are correctly handled. It offers a simpler and more compact design, with fewer filters, and a lower bill of materials. Using a direct conversion receiver such as the CMX994 series, which has very low second order intermodulation products, ensures that DC offsets are naturally kept to a minimum. Secondly, using a technique of measuring and compensating for any offsets that do occur, such as the method described here, will ensure that the benefits of direct conversion can be achieved without any detrimental effect on the quality of the received, demodulated signal.