CS2100 Clock Circuit IC

Featuring a Clock Generator and Clock Multiplier/Jitter Reduced Frequency Synthesizer for Ethernet AVB Networks

1. Introduction

Automotive infotainment audio and video features such as DVD playback, remote amplifiers, rear seat entertainment, cameras and navigation have created the need for a time-synchronized automotive network. Point-to-point solutions require expensive and complex cabling and alternative networking architectures such as MOST (Media Oriented Systems Transport) are based on proprietary standards and offer only a single source for hardware.

Audio Video Bridging (AVB) is an enhancement to the Ethernet suite of open standards. It provides network time synchronization and a transport protocol that enable the network to handle time-sensitive audio-visual (AV) data. As an example of the importance of precise time synchronization, consider a movie that is playing in a vehicle that has two video displays plus audio playing on the vehicle's speakers. Ethernet AVB allows lip-synced playback of AV content across all of the devices.

Ethernet AVB leverages the existing Ethernet hardware and software ecosystem and adds the high-reliability, flexibility and precise time synchronization required by audio and video applications.

AVB achieves precise time synchronization by utilizing IEEE 802.1AS Precision Time Protocol (PTP). The PTP protocol is distributed and specifies how the real-time clocks in the system synchronize with each other. The master clock establishes the reference time for the network. Synchronization is achieved by precisely time-stamping packets as they leave the master and arrive at each slave node. PTP measures and compensates for any queuing or transmission delays. In this way, each slave node maintains a clock that is synchronized to the master clock. The PTP slave clock is generally operating at a low frequency, often 1 kHz. Audio converters require an input clock at a significantly higher rate, commonly 12.288 MHz. Each node requires a high-factor clock multiplier with low-frequency reference compatibility. In addition, high-fidelity playback requires jitter performance <120 picosecond RMS. The CS2100 is a unique solution that provides a combination of low input frequency clock multiplier with low jitter and low cost. This combination meets the requirements for Ethernet AVB audio nodes.

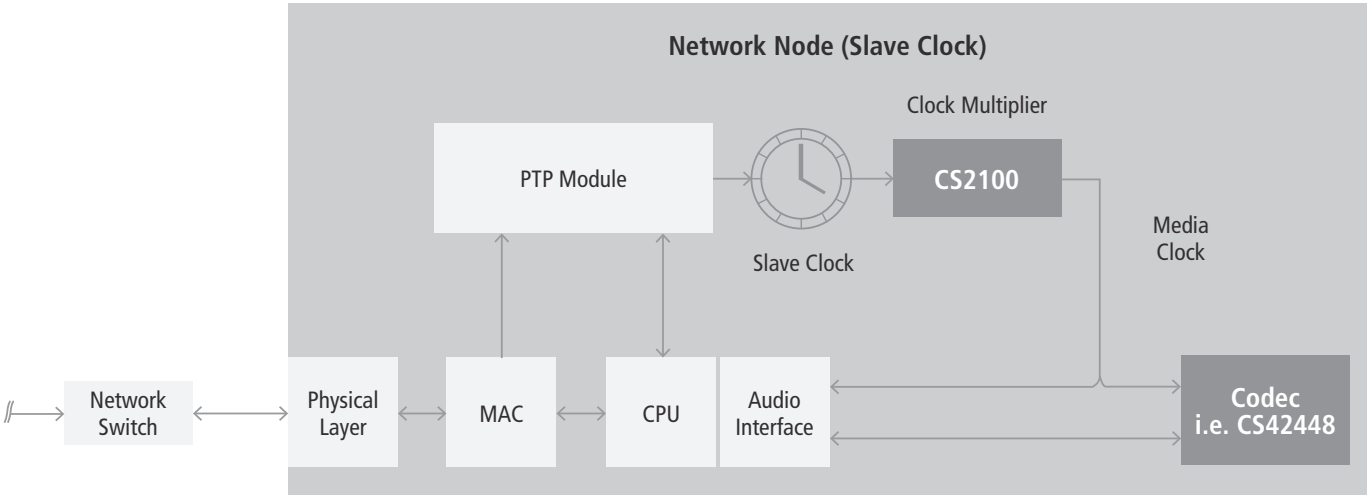

***Figure 1-1:** Generating media clock with the CS2100 enables a tight architectural combination of hardware and software elements*

The CS2000 family of devices includes the CS2000, CS2100, CS2200 and CS2300. A feature comparison for these devices is shown in Table 5-1. The CS2100 is an optimized solution for generating the media clock that is in step with the global master clock. The flexible architecture combined with convenient configuration options makes the CS2100 the optimal solution to generate an Ethernet AVB slave node media clock.

2. Ethernet Time Synchronization Principles

The high volume deployment of Ethernet networks drives economies of scale and opens new opportunities. Basic building blocks to implement the standards are widely available, and a simplified block diagram of the lower layers is shown in Figure 2-1. The Media Access Controller (MAC) is often implemented in a standards-based device. The higher layers of the protocol stack are typically handled by some type of processor labeled as Operating System (OS).

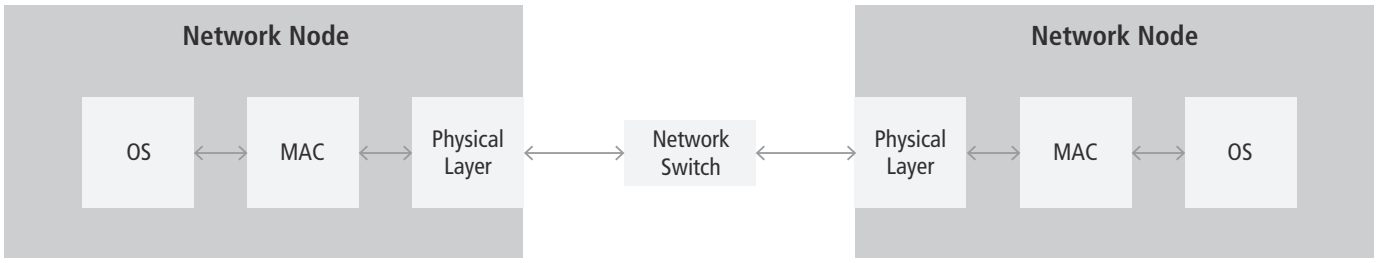

***Figure 2-1:** Example Ethernet implementation block diagram*

Data is transported across a legacy Ethernet link as a packet with no concept of a network clock. The packet based messaging architecture does not rely on specific timing and the initial standards do not enable precise synchronization of clocks. To address the time-aware requirements of measurement and control applications, new standards were created that introduce a hierarchical master-slave architecture for clock distribution. The Precision Time Protocol (PTP) defined in the IEEE 1588 standard is used to synchronize clocks throughout a computer network.

Synchronous time information is distributed hierarchically from a master clock, along with carefully timestamped packets, to one or more slave clocks. Figure 2-2 is a high level representation showing a master clock and a slave clock in a simplified network.

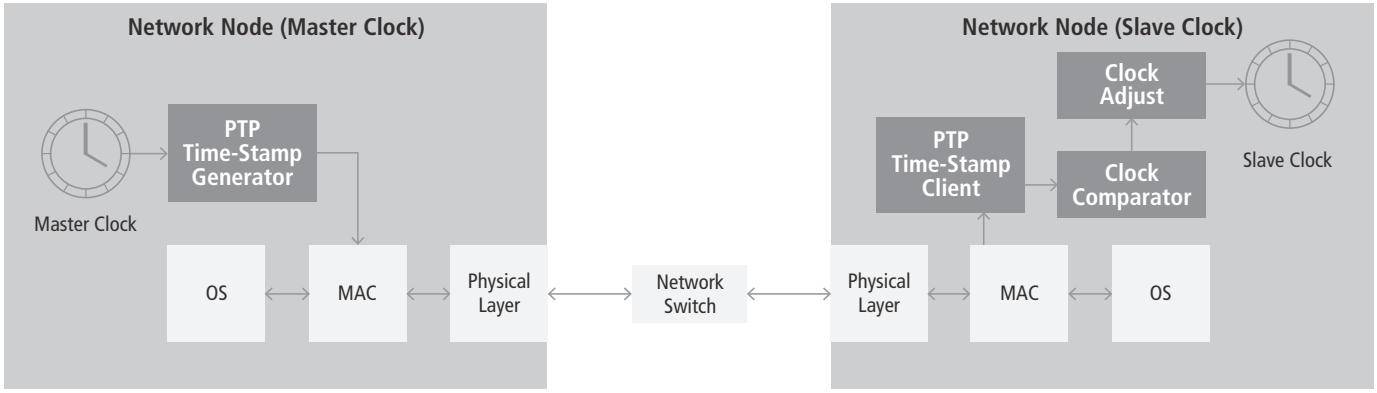

***Figure 2-2:** Simplified representation of synchronizing clocks using PTP*

The PTP protocol is a distributed protocol that specifies how the real-time clocks in the system synchronize with each other. Synchronization is achieved by exchanging PTP timing messages, with the slaves using the timing information to adjust their clocks to the time of their master in the hierarchy. The master clock determines the reference time for the entire system. Creating time-sensitive networks using these standards brings benefits to many industries such as industrial controls. Highly-integrated ICs are available from many suppliers to implement these standards for network synchronization. Although these devices were not designed for the end application of audio distribution they can still be useful in AVB systems as described in the next section.

3. Ethernet Audio/Video Bridging (AVB)

Ethernet AVB is a set of non-proprietary networking standards that take advantage of the PTP protocol to create packet-based synchronized networks that are ideal for streaming media. It is implemented with relatively small extensions to the previously existing standards. This minimal change approach makes it possible for AVB devices to share the same network as non-AVB devices. The enhancements provide highly-reliable delivery of low-latency, synchronized audio and video.

Time-aware networks are not required for streaming media to a single consumer (one renderer). For example, the methods used for on-demand Internet streaming media are sufficient for one user, but are not satisfactory for synchronized playback on multiple monitors in a large room. With the goal of creating more universal applications of multimedia transport, Ethernet AVB standards insure that multimedia devices can be networked with common cabling (such as CAT-5) and allow multiple users to share synchronized content. And along with sharing content, functionality such as play/pause and volume control is made available across the network. Sophisticated audio networks with this type of performance are common today in theme parks and recording studios.

3.1 Automotive Telematics and Infotainment Networks

A crucial feature in automotive infotainment systems is the seamless integration of audio/video interfaces into the network interface controllers. Ethernet AVB delivers the increased bandwidth and flexible topology required in the vehicle to address new requirements.

As an example of the importance of shared time, consider a movie that is playing in a vehicle that has two video displays while the audio is playing on the vehicle's speakers. Ethernet AVB allows lip-synced playback of AV content across multimedia devices. The speaker drivers (i.e. amplifiers) can be distributed throughout the vehicle because real-time audio is distributed across the network. New video applications such as high resolution image recognition in advanced driver assistance systems are supported. Ethernet AVB fulfills the automotive requirements of cost, scalability, maturity, future-proof design and security. Automobile manufacturers and original equipment manufacturers are designing Ethernet AVB systems for vehicles today.

4. Media Clock Timing Solution

The block labeled Clock Adjust in Figure 2-2 is typically implemented in firmware along with hardware assist circuits in a standards-based device. It is desirable to update the clock adjust loop at a low frequency to minimize the processing burden.

4.1 Audio Clock (MCLK) Generator

Most audio converters require a low-jitter clock signal (MCLK) that is an even multiple of the audio sample rate and is synchronous with the digital audio interface signals (SCLK, LRCK). For example, when using a 48 kHz sample rate for digital audio, a typical converter will require an MCLK frequency of 12.288 MHz (12.288 MHz = 48 kHz hi-fi sample rate x 16-bits x 16 channels TDM).

Cirrus Logic provides the solution for generating MCLK in audio network applications with the CS2100 as shown in Figure 4-1.

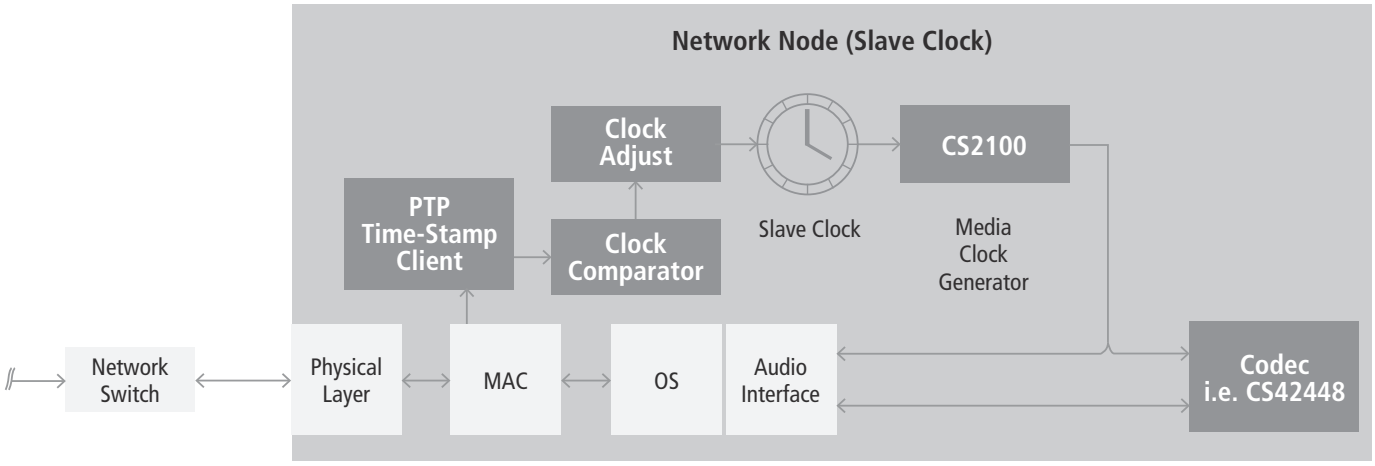

Figure 4-1: ***CS2100 solves the media clock recovery challenge***

In a typical audio endpoint application, the synchronized slave clock provides a reference to the CS2100. The CS2100 locks to this reference and generates the low-jitter MCLK with the proper time information.

As an example, the slave clock may be designed to generate a PTP clock at 1 kHz. The CS2100 is configured to multiply that input to 12.288 MHz as an input to the codec. The unique architecture of the CS2100 also cleans jitter from the PTP clock to produce a clock with 50 ps RMS baseband jitter. High-fidelity audio requires jitter <120 picosecond RMS.

4.2 Design Architecture

The CS2100 architecture includes a Delta-Sigma Fractional-N Frequency Synthesizer and a Digital PLL as shown in Figure 4-2.

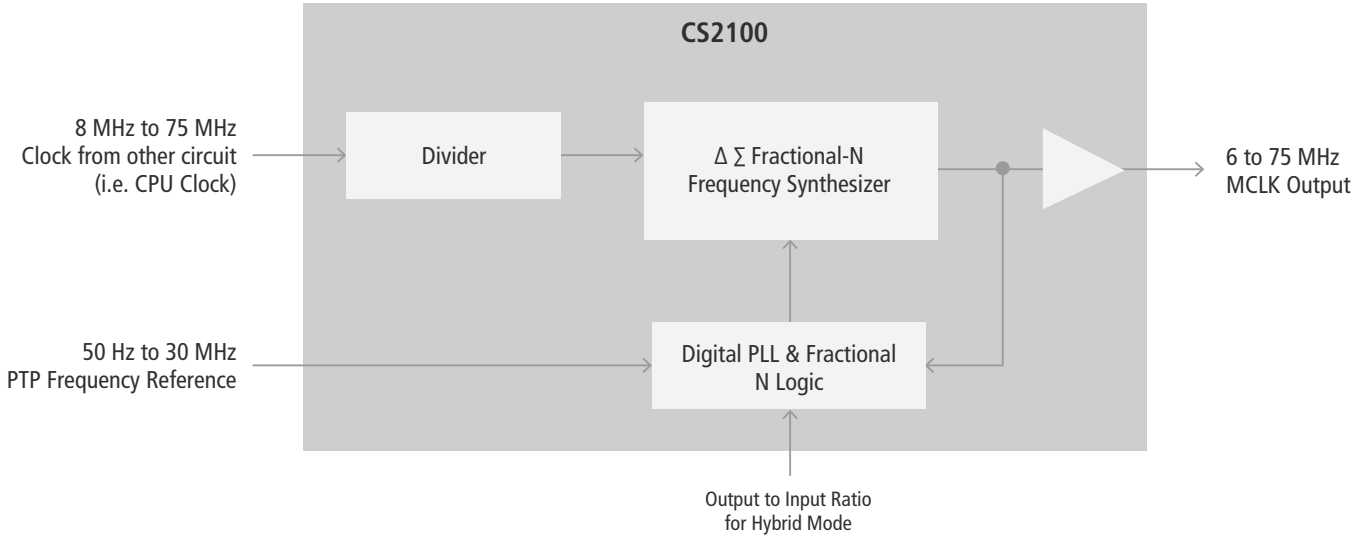

Figure 4-2: ***CS2100 generates the required MCLK frequency based on the PTP clock as a reference***

This hybrid architecture generates a clean MCLK output when locked to the PTP frequency reference because it supports independent analog and digital loop filters. The CS2100 uses an adaptive digital loop filter bandwidth to optimize lock-time and jitter attenuation.

The architecture of the CS2100 has more capability than the classical PLL that may be integrated with a codec to generate MCLK from the incoming left-right clock. First, those classical PLL solutions cannot be used with a low frequency reference input. A typical minimum frequency is 32 kHz, compared to a minimum of 50 Hz for the CS2100. And secondly, the hybrid architecture gives the designer greater control of system performance.

4.3 Optimized for Ethernet AVB Applications

This unique architecture provides an optimized solution for generating MCLK in an audio network. Other devices such as timing PLLs designed for telecom networks include multiple outputs and other features that are not required in the Ethernet AVB application. In addition, these devices from other vendors are typically much more expensive without bringing added benefit. And the CS2100 has the unique ability to support 50 Hz to 30 MHz input frequency range and thereby allow the PTP clock to operate at an optimal frequency. Operating the slave clock at a low frequency makes it possible to operate the PTP clock adjust loop at a low frequency resulting in lower processor overhead.

Implementing a timing loop in software to generate the sample rate clock would place an unnecessary burden on the network device's host controller. For example, common audio applications use "Class A" streaming, which has a measurement interval specified as 125 µs, equivalent to 8 kHz. This is valid for a single stream only, and every Ethernet frame would need to be evaluated at that rate in order to maintain an isochronous connection. The implementation of interrupt services in software at a speed of 8 kHz to meet the above requirement would be a severe challenge for a network device's host controller running a preemptive multitasking operating system.

4.4 Isolating Media Clocks with System Partitioning

At the system level it may seem desirable to operate the recovered PTP clock at the MCLK frequency. This would severely impact the analog performance of the audio converter, and consequently the system's audio quality in terms of THD+N and dynamic range. Partitioning the design to keep the media clock generator separate allows the designer to focus on generating a low frequency PTP clock without placing emphasis on jitter. The CS2100 multiplies the PTP clock to the required MCLK frequency and reduces the jitter as shown in Figure 4-3.

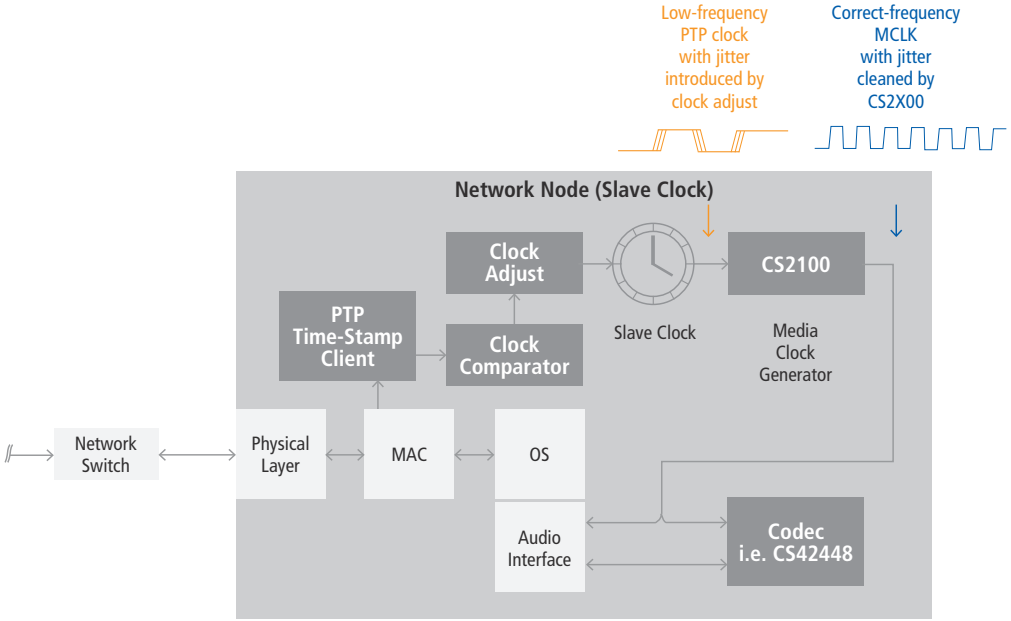

***Figure 4-3:** Partitioning the system allows the CS2100 to isolate the media clock and keep it clean*

The synchronization of distributed clocks requires a continuous process. This is due to the fact that the frequency sources used for clocks have limited precision and the rate of drift changes over time and temperature.

Consider an example when a node has an unstable clock. Perhaps the frequency is changing rapidly because of temperature change. The clock adjust circuit will adjust the local clock to match the new frequency, but this will temporarily cause a phase difference between the master and the local clock. The frequency can be adjusted more rapidly, but this creates a higher frequency jitter in the clock signal.

Employing the CS2100 as the media clock generator allows partitioning the blocks according to function. And it improves the ability to support multiple media clocks on the same Local Area Network (LAN). The AVB network inherently supports an arbitrary number of different media sample rates and clock sources because the destination devices will each synchronize to their corresponding source device. And partitioning the media clock generator as a separate device improves the ability to adapt to different sample rates. Support for various sample rates is a standard feature of the CS2100 devices provided by the Ratio Modifier register as described in the product data sheet.

4.5 Industry Group Certification

Ethernet AVB standards assist manufacturers to produce products that will operate properly with other manufacturer's products. The AVnu Alliance is an industry group that is dedicated to promoting the standard and has created a certification process. The first certified AVB audio endpoint reference platform is one of the products that has passed all testing for AVnu certification and is designed using the CS2100.

5. Flexible Product Offerings

The CS2000 family includes four devices as shown in Table 5-1. Each of the devices has an output frequency range of 6 to 75 MHz and is available in a 10-pin MSOP package.

Product	Frequency Synthesizer/ Clock Generator	Clock Multiplier/ Jitter Remover	Input Frequency Range	Reference Frequency Range
CS2000	Yes	Yes	50 Hz to 30 MHz	8 to 56 MHz
CS2100	—	Yes	50 Hz to 30 MHz	8 to 56 MHz
CS2200	Yes	—	—	8 to 56 MHz
CS2300	—	Yes	50 Hz to 30 MHz	Internal

***Table 5-1:** CS2000 family sorted by features*

The CS2100 is the ideal low-cost solution for Ethernet AVB nodes. The CS2000 includes additional registers to support frequency synthesis. The CS2200 does not support locking to an external frequency reference and therefore is not applicable in Ethernet AVB applications. The CS2300 includes an internal timing reference clock source, so no external crystal or clock source is required. The CS2300 can be used in Ethernet AVB nodes where no external clock source is available.

Each of the devices is available with two different methods for configuration. Select the configuration method that best meets your application needs by ordering the device with the associated suffix, either -CP or -OTP.

1. The CS2X00-CP is configured using the serial Control Port (CP). This provides the designer with many configuration options as detailed in the device data sheet.

2. The CS2X00-OTP device includes internal One Time Programmable (OTP) memory. The memory is programmed once during manufacturing, and then the device will be configured and to run in a stand-alone mode. The OTP devices have three mode pins that are used to select operational parameters.

5.1 Automotive Grade

The CS2000 family is ideal for use in automotive applications. Table 5-2 shows the available temperature ranges.

Product	Description	Order # Suffix	Grade	Temperature Range
CS2000	Full-featured clocking device	-CZZ	Commercial	-10°C to +70°C
		-DZZ	AEC-Q100 GRADE 3	-40°C to +85°C
		-EZZ	AEC-Q100 GRADE 2	-40°C to +105°C
CS2100	Clock Multiplier/Jitter Reducer	-CZZ	Commercial	-10°C to +70°C
		-DZZ	AEC-Q100 GRADE 3	-40°C to +85°C
		-EZZ	AEC-Q100 GRADE 2	-40°C to +105°C
CS2200	Clock Synthesizer	-CZZ	Commercial	-10°C to +70°C
		-DZZ	AEC-Q100 GRADE 3	-40°C to +85°C
		-EZZ	AEC-Q100 GRADE 2	-40°C to +105°C
CS2300	Clock Multiplier/Jitter Reducer with internal oscillator	-CZZ	Commercial	-10°C to +70°C
		-DZZ	AEC-Q100 GRADE 3	-40°C to +85°C

Table 5-2: Temperature range information

6. Summary

The CS2100 provides a unique, low cost combination of low-input frequency reference, high factor clock multiplier and extremely low jitter. This makes it the ideal clocking solution for Ethernet AVB.

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