White paper:

Meeting New NOR Memory Design Requirements with Cypress' HyperBus™ Interface and Synopsys DesignWare® IP

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Introduction

NOR Flash memory was first introduced in the late 1980s with a parallel interface: one bus for data/command (x8-bit or x16-bit) and a separate address bus with a bit-width that was proportional to the Flash density (e.g. 22 address inputs for a 64 Mb Flash density).

The performance of this interface was enough to meet the requirements of end applications like consumer set-top boxes and ADSL routers. The high pin count of the interface (e.g. 46 pins for 64 Mb density considering all inputs and configuration pins) was also acceptable, given its large package size and the relatively low number of peripherals connected to them.

In the early 2000s, the shift to more advanced logic geometries reduced SoC die size and, in turn, its package size and allocated pins. This compact silicon footprint, coupled with the need to reduce the printed circuit board (PCB) size for portable devices, led to the introduction of a new type of NOR Flash memory based on the popular Serial Peripheral Interface (SPI).

SPI's low pin-count (4 active pins), an average performance of 6.25 MB/s with single I/O interface, and availability of low densities made SPI NOR memory a viable option for many applications. As SPI NOR was predominantly used to store parameters rather than application code, it provided an excellent complement to Parallel NOR Flash.

Over time, users wanted to replace Parallel NOR Flash memory entirely with SPI NOR memory. This led to the development of higher density SPI NOR devices that also offered much higher throughput by going from a single I/O to a dual I/O – and ultimately quad I/O – interface.

By 2010, the standard performance of SPI NOR Flash memory reached 26 MB/s (e.g. 104 Mhz with a quad I/O interface). The transition from Parallel NOR to SPI NOR was well under way.

However, there was a need for even higher data rates. For example, system requirements for faster boot time and eXecute-In-Place (XiP) capabilities mandated a performance jump enabled by the SPI NOR protocol running on Double Data Rates (DDR), hence doubling throughput to 52 MB/s.

The need for higher performance and throughput continued to be driven by the increasing code size of applications and requirements to execute in the same amount of time or even faster. The industry pushed the DDR frequency to 80 Mhz, enabling 80 MB/s throughput with a quad I/O interface.

For applications such as entry- and mid-level automotive clusters, some SoC designers were looking at fetching images directly from Flash without going through an expensive external DDR DRAM. To achieve this, they needed extra performance for SPI NOR Flash. Such SoC designers chose to instantiate two SPI controllers and, accordingly, two SPI NOR Flash in quad I/O and 80 Mhz DDR.

The industry reached its performance limits with QSPI NOR Flash. This had the minimum set-up and hold timing that could be handled by a memory controller with a maximum number of acceptable Flash components for code execution. But Cypress, working very closely with SoC designers to understand their system performance requirements, anticipated the need for higher performance NOR Flash. To meet this need, the company developed the innovative x8-bit Flash HyperBus interface and brought it to market in 2014. The Cypress HyperBus Interface increases SPI from x4-bit to x8-bit. This meets the low pin-count requirements that SoCs need, given their advanced process geometry and small package size on which any additional pin has a cost impact. HyperBus uses an innovative architecture to increase the frequency up to 200 Mhz DDR in its current generation: Semper™ Flash, which was launched in May 2018.

With the introduction of HyperBus, a new class of high-performance NOR Flash solutions were ushered into the market enabling instant-on functionality for Industry 4.0/Smart Factory applications, as well as autonomous driving applications. Figure 1 illustrates the evolution of NOR Flash memory.

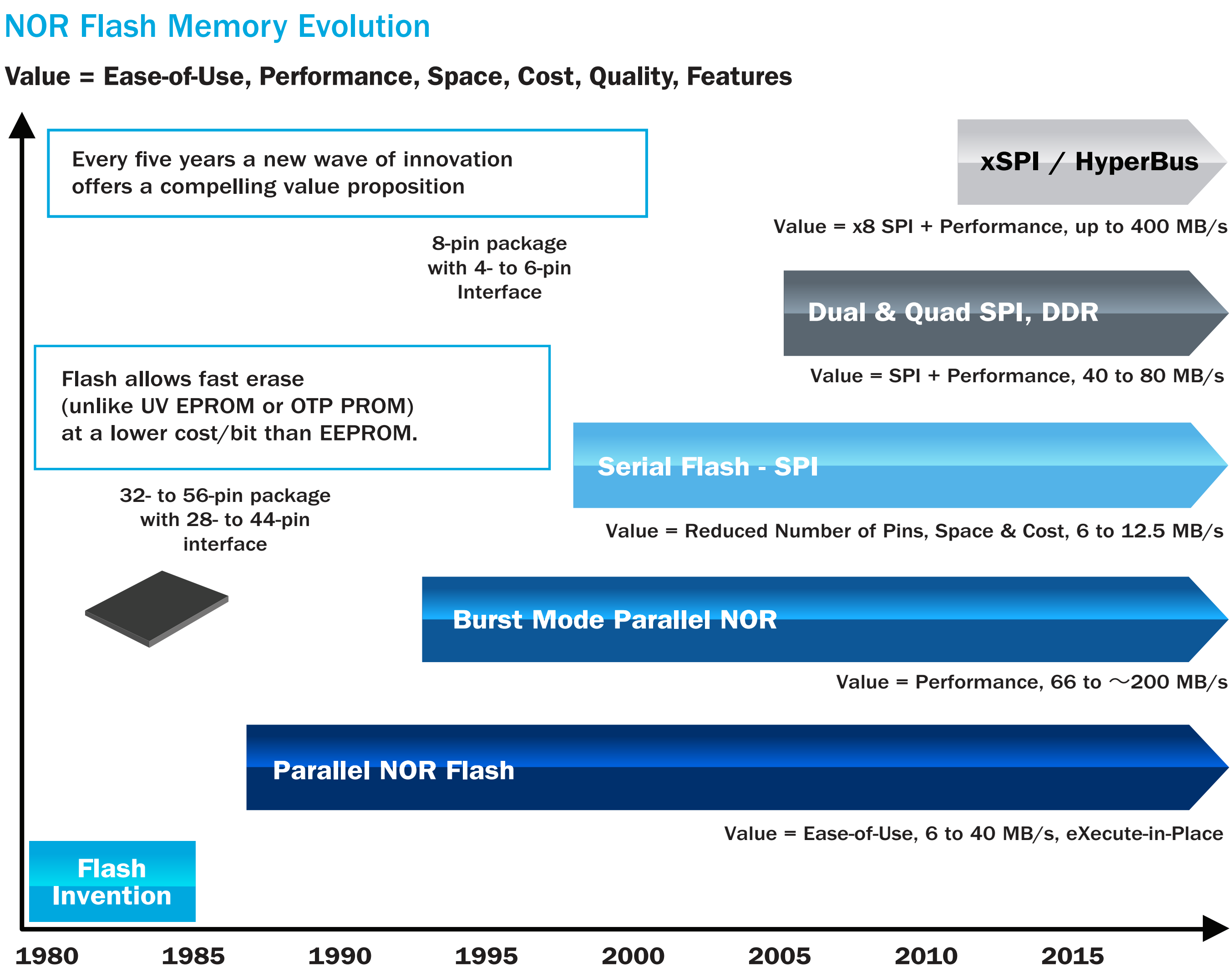

Figure 1: The Evolution of NOR Flash Memory

The HyperBus is a x8 serial interface designed to support more than three-times faster read performance compared to conventional NOR Flash memory using only 12 mandatory control and data signals for read and write transactions. Figure 2 illustrates HyperBus signaling from the viewpoint of a host controller. Figure 3 shows HyperBus signaling from the viewpoint of a slave device.

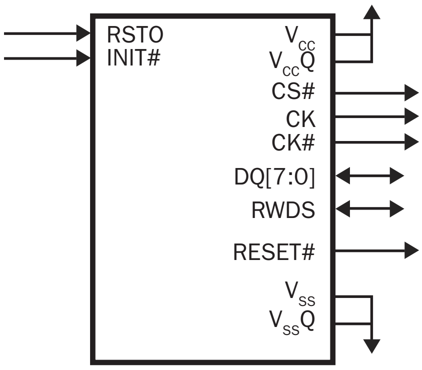

Figure 2: HyperBus signaling from the viewpoint of a host controller.

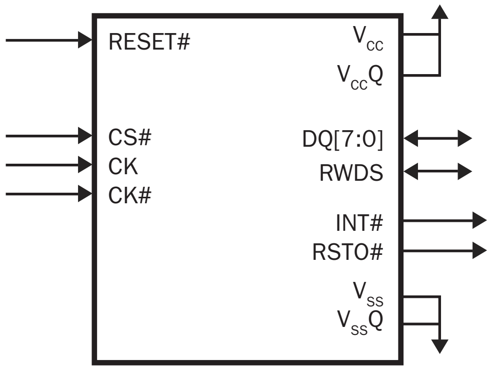

Figure 3: HyperBus signaling from the viewpoint of a slave device.

The 12 control and data signals are:

- CS#: Chip Select. Bus transactions are initiated with a High-to-Low transition. Transactions are terminated with a Low-to-High transition.
- CK (Clock Signal) and CK# (Clock signal on opposite phase): A command, address, and data output with respect to the crossing of the CK and CK# signals. CK# is used on 1.8V devices only; 3.0V devices use a single-ended clock.
- DQ [7:0]: Data Input/Output: Command, address, and data are transferred on these signals during read and write transactions.
- Read Write Data Strobe (RWDS): An output from the HyperBus device indicates when data is being transferred from memory to the host. RWDS is referenced to the rising and falling edges of CK during the data transfer portion of read operations. Command, address, and write-data values are center-aligned with the clock edges. Read-data values are edge-aligned with the transitions of RWDS. This signals to help the host to calibrate the read data accurately.

There are three optional signals to reset a slave device – RESET# [Hardware Reset] and RSTO# [Reset Output] – or to transfer an interrupt notification to master [INT#].

HyperBus Controllers

HyperBus is a versatile interface that supports both a NOR Flash, called HyperFlash, and a RAM called HyperRAM. HyperRAM has a DRAM core and a HyperBus interface. The additional latency needed to refresh the DRAM core is indicated to the host due to the RWDS signal.

With HyperBus, a complete memory subsystem (NOR and RAM) can be supported by a single, low pin-count interface and memory controller. Requiring just 13 pins (12 pins of HyperBus interface plus an extra Chip Select [CS2]), this flexible interface elegantly removes the burden of additional costly DRAM memory controllers with high pin-count interfaces.

Since HyperBus is a new interface and protocol, it requires new memory controllers. Unfortunately, SoC designers would rather not spend time developing IP blocks that do not directly contribute to product differentiation, and they don't want to have to deal with inherent design risks and unforeseen peripheral compatibility issues that are common to new IP development. They would prefer to focus on enhancing their core architecture design and fine-tuning their software. To minimize investment risks, many SoC designers rely on third-party IP providers for proven and tested IP for memory controllers, such as Synopsys DesignWare IP.

Synopsys is a leading memory controller IP provider for SPI. The Synopsys DesignWare Controller IP for Synchronous Serial Interface supports all the key features of SPI, offers multiple device roles (master, slave), and provides both AHB and APB application interfaces. The IP supports dual/quad or octal SPI with SDR and DDR modes of operations. The configurable IP can dynamically switch from the HyperBus mode of operation to normal mode, is fully compliant with the HyperBus protocol, and provides support for eXecute-In-Place (XIP) and HyperFlash devices.

Users can enable the HyperBus feature in the Synopsys DesignWare Controller IP for Synchronous Serial Interface using the SSIC_HYPERBUS_EN configuration parameter. Once the HyperBus feature is enabled in Synopsys' IP, the CTRLR0.SPI_HYPERBUS_EN register bit is used to program the DesignWare IP as a HyperBus master. Users can configure wait cycles, type of transaction (read/write), and data frame size in the SPI_CTRLR0.WAIT_CYCLES, CTRLR0.TMOD, and CTRLR0.DFS fields, respectively. Figure 4 shows the signal connections from the Synopsys DesignWare IP master with a typical HyperBus slave device.

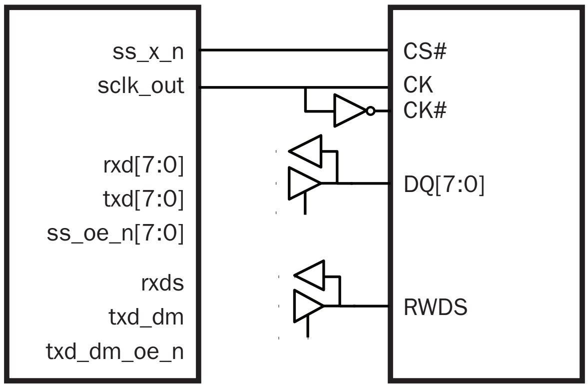

Figure 4: Signal connections from the Synopsys DesignWare IP master with a typical HyperBus slave device.

Optional signals to reset (RESET# [Hardware Reset] and RSTO# [Reset Output]) or transfer an interrupt notification to master [INT#] can be connected via glue logic.

As additional memory suppliers have entered the market, each has proposed highly customized x8 high-performance products. Such fragmentation of the market has made it difficult for controller and chipset manufacturers to support all x8 high-performance NOR Flash interfaces. This has placed the burden of providing a system solution with interoperable x8 serial NOR Flash on the memory controller to support multiple Flash interfaces with customized device drivers for each Flash interface. Such design complexity resulted in slowing the adoption of x8 high-performance NOR Flash, as some chipset designers and customers opted to wait until an industry standard was released.

The new JEDEC eXpanded SPI (xSPI) standard, ratified by JEDEC in June 2017, defines a minimum set of requirements for compatibility of high-performance x8 serial NOR Flash interfaces. With this standard, controller and chipset manufacturers are now able to design a universal memory controller.

The inclusion of the HyperBus interface in the JEDEC xSPI standard simplifies support of HyperBus-based memories for SoC providers and system designers developing applications that require high-performance x8 NOR Flash.

Cypress' new Family of Semper Flash with the HyperBus interface is fully compliant with the JEDEC xSPI standard. Figure 5 shows a comparison of system solutions for x8 NOR Flash and Semper xSPI with a HyperBus interface.

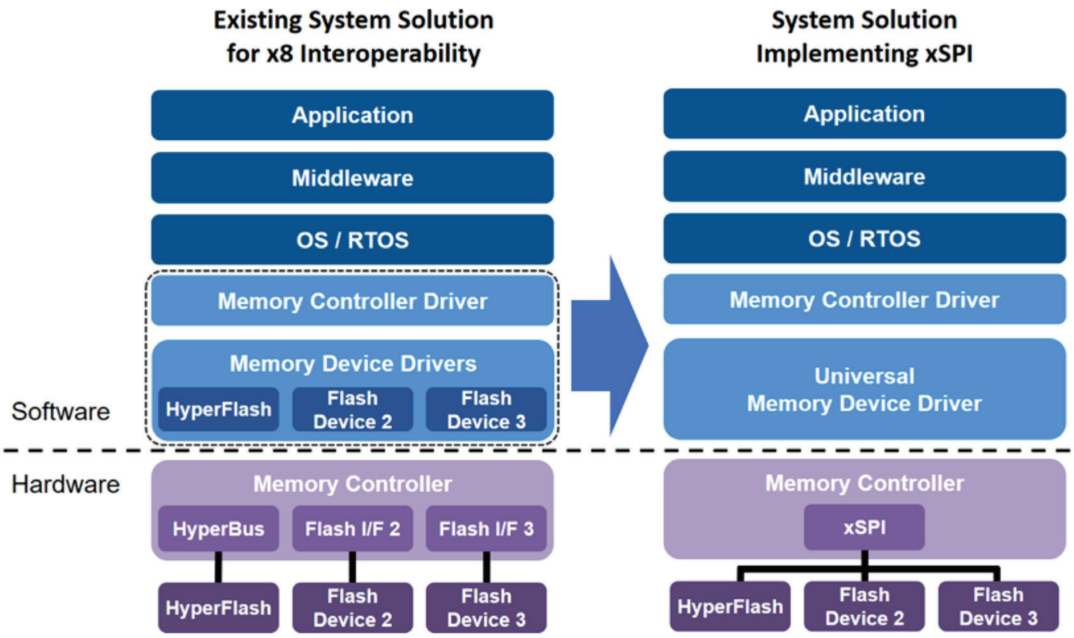

Figure 5: Comparison of system solution for x8 NOR Flash and Semper xSPI with HyperBus interface.

With the release of the xSPI specification, memory controller design is greatly simplified. Instead of designing memory controllers that support multiple interfaces, a memory controller designed to the xSPI specification guarantees compatibility with xSPI-compliant Flash.

Synopsys DesignWare Controller IP for Serial Synchronous Interface is in compliance with the xSPI specification and Synopsys will continue to work closely with JEDEC to comply with future updates.

To give additional flexibility to customers and designers, HyperBus devices (HyperFlash and HyperRAM) are available in a 24-ball FBGA package common to existing Quad SPI and Dual Quad SPI NOR Flash memories. A single PCB footprint layout can be used for Quad SPI, Dual Quad SPI, and HyperBus devices, giving system designers flexibility in determining which solution to use based on its system performance requirements. Figure 6 shows the details on the common memory footprint to accommodate one Quad SPI NOR Flash, Dual Quad SPI NOR Flash, HyperFlash, and HyperRAM.

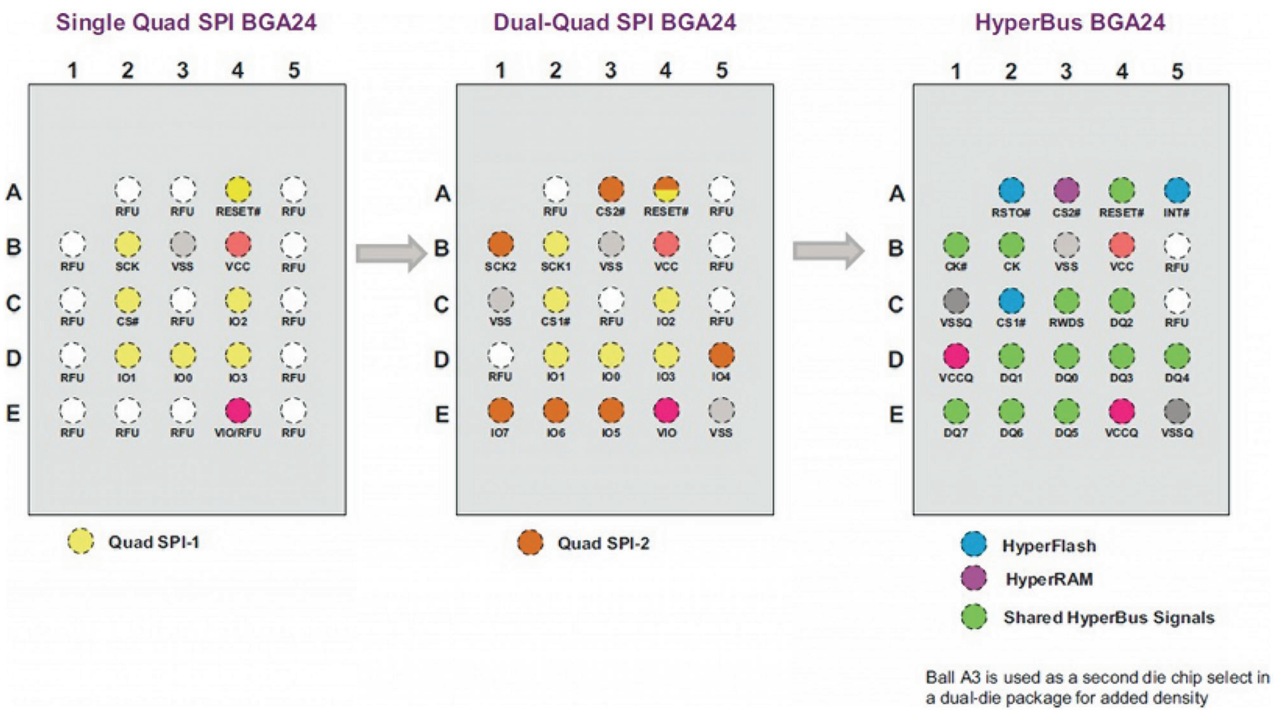

Figure 6: A common memory footprint accommodates one Quad SPI NOR Flash, Dual Quad SPI NOR Flash, HyperFlash, and HyperRAM.

HyperFlash Memory for Automotive Applications

Cypress created and introduced the HyperBus interface, and has developed developed HyperFlash Memory Products that come with differentiated features that enhance the Functional Safety (FuSa) of systems. FuSa is a critical aspect of automotive applications, especially Advanced Driver Assistance Systems (ADAS) and autonomous driving platforms which require a high Automotive Safety Integrity Level (ASIL) to guarantee the safety of the system. FuSa also applies to critical industrial applications such as factory automation, where Safety Integrity Level (SIL) is an important criterion.

HyperFlash Memory products offer several differentiating features, including:

- **Internal ECC (1-bit ECC / 2-bit EDC):**
  - Internal error code correction (ECC) guarantees protection against a bit flip within the memory array. Statistical monitoring of ECC correction occurrences and determination of the location in the memory array where ECC correction has been applied can be monitored through dedicated the Status Register in the HyperFlash.
  - ECC occurrence or uncorrectable 2-bit errors can be flagged externally through the optional INT# pin of the HyperFlash interface, providing awareness to the SoC and Safety action and correction to be performed by the system.
  - Furthermore, embedded ECC enhances the reliability (Failure In Time: FIT level) of the Flash Memory device and counters the effects of alpha particles, which can create bit flips in Flash memory with particularly critical effects in the case of automotive applications.
  - ECC within the memory array is transparent to the user and requires no action to be applied.

- **EnduraFlex**:
  - A Cypress Flash feature developed for devices based on MirrorBit (2-bit-per-cell) 45nm technology (i.e. Cypress' new Semper Flash family).
  - EnduraFlex relies on an internal wear-leveling mechanism which tremendously increases the Program / Erase (P/E) Cycle endurance from a typical 100K P/E cycle by a factor of 12x to a 1.2M P/E cycle. This also increases the typical data retention from 20 years to 25 years.
  - Designers can partition the Flash into up to 5 different partitions, each configurable for "High Endurance" (1.2M P/E cycle) or "High Data Retention" (25 years).

Conclusion

Design requirements like high throughput, high-density, and low pin-count for SoCs across a wide range of applications is forcing designers to consider memory solutions that meet or exceed such requirements. NOR Flash, with its 46 pins for 64 Mb density, was a sufficient option before SPI became a more viable memory option due it is low pin-count, performance at 6.25 MB/s, and low densities. SPI NOR memory offers much higher throughput by evolving from a single I/O to a dual I/O, and ultimately to a quad I/O interface.

Cypress has developed the innovative x8-bit HyperBus Flash interface that supports both a NOR Flash, called HyperFlash, and a RAM called HyperRAM. Since HyperBus is a new interface and protocol, it requires new memory controllers. Controllers that are proven, compliant, and seamlessly interoperable with the Cypress interface are available today. Synopsys' DesignWare Controller IP for Serial Synchronous Interface, supporting the Cypress HyperBus interface, provides a proven solution, compliant with Cypress' HyperBus memories (65-nm MirrorBit, and 45-nm Semper Flash). HyperBus enables SoC designers to benefit from low pin-count, high performance memories with up to 400 MB/s throughput (200 Mhz DDR) for both NOR (HyperFlash) and RAM (HyperRAM) devices.

For more information on Cypress' Semper NOR Flash solution, please visit:
https://www.cypress.com/event/semper-nor-flash

For information on Synopsys DesignWare Controller, please visit:
https://www.synopsys.com/designware-ip/interface-ip.html

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