



Process Change Notification Form

PCN Number:	PCN_0243
Date of Notification:	November 21, 2008
Cirrus Logic P/N(s):	CS3308-CQZ, CS3308-CQZR, CS3318-CQZ, CS3318-CQZR
Date PCN Effective:	February 20, 2009
Reason for Change:	<input checked="" type="checkbox"/> Design /New Rev. <input type="checkbox"/> Fab Site <input type="checkbox"/> Fab Process <input type="checkbox"/> Additional Fab Source <input type="checkbox"/> Assembly Site <input type="checkbox"/> Assembly Process <input type="checkbox"/> Additional Assembly Source <input type="checkbox"/> Other (specify)
Description of Change:	<input checked="" type="checkbox"/> Fix errata <input type="checkbox"/> Yield enhancement <input type="checkbox"/> Fix known bug <input type="checkbox"/> Performance Improvement <input type="checkbox"/> Other **Please see pages below** Revision C0 backward compatible to Revision B0
Cirrus Logic P/N Change:	<input type="checkbox"/> Yes, New Part Number: <input checked="" type="checkbox"/> No
Pack Mark Change:	<input checked="" type="checkbox"/> Yes <input type="checkbox"/> No If Yes, briefly explain: YFWAB0 to YFWAC0 <i>[Any Fab, Assembly, or Design changes results in pack mark changes, please provide detail]</i>
Lot Effective Date:	0826 for CS3308-CQZ/C0 0744 for CS3318-CQZ/C0 <i>[Contact the area sales representative for availability of samples if applicable]</i>
Quality & Reliability impact:	**Please see pages below** Qualification Data: <input checked="" type="checkbox"/> Required <input type="checkbox"/> Not Required
Datasheet Change Required?	<input type="checkbox"/> Yes <input checked="" type="checkbox"/> No If Yes, briefly explain:
Software Change Required?	<input type="checkbox"/> Yes <input checked="" type="checkbox"/> No If Yes, briefly explain:

Errata: CS3308 Rev. B0

Rev. B0 Silicon (Reference CS3308 Datasheet)

- ◆ To achieve the specified analog performance, the following sequence must be written to the CS3308 internal registers following the release of reset and prior to any other register writes:
 1. Write 0x99 to register 0x00.
 2. Write 0x87 to register 0x1D.
 3. Write 0x42 to register 0x1F.
 4. Write 0x00 to register 0x00.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to <http://www.cirrus.com/corporate/contacts/sales.cfm>

Errata: CS3318 Rev. B0

Rev. B0 Silicon (Reference CS3318 Datasheet)

- ◆ To achieve the specified analog performance, the following sequence must be written to the CS3318 internal registers following the release of reset and prior to any other register writes:
 1. Write 0x99 to register 0x00.
 2. Write 0x86 to register 0x1D.
 3. Write 0x02 to register 0x1F.
 4. Write 0x00 to register 0x00.

Contacting Cirrus Logic Support

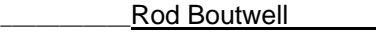
For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
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RELIABILITY QUALIFICATION REPORT

Report Date: 11/17/2008

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Reliability Report: QRR081106

<p>Subject/Purpose: This is to qualify the CS3308-CQZ/C0 and CS3318-CQZ/C0 devices manufactured at MagnaChip (F) and assembled in the Pb-free 48LQFP package at Siliconware (Taiwan).</p>	<p>APPROVALS: <div style="text-align: center;">  Reliability Engineering </div> </p>
<p>Results: Qualification successful.</p>	<p>STATUS: Complete - Pass</p>

<u>Stress</u>	<u>Conditions</u>	<u>Method</u>	<u>Duration</u>	<u>Lot</u>	<u>Results (Fail/Sample)</u>
HTOL	125 °C	JESD22-A108	500 Hours	1	0/77
1203-1 (Rev. A0)	5.25 Volts		1000 Hours	1	0/77
1214-1 (Rev. B0)	-5.25 Volts				
QJ1435 (Similarity)	3.5 Volts		24 Hours	2	0/77
	Dynamic		48 Hours	2	0/77
			500 Hours	2	0/77
			1000 Hours	2	0/77
	125 °C		96 Hours	3	0/77
	9.45 Volts		500 Hours	3	0/77
	-9.45 Volts		1000 Hours	3	0/77
	3.5 Volts				
	Dynamic				
	125 °C				
	3.6 Volts				
	12.6 Volts				
	Dynamic				
ESD Human Body Model QJ1345	25 °C	JESD22-A114	2000 Volts	1	0/5
ESD CDM (Charged Device Model) QJ1516	25 °C	JESD22-C101	500/750 Volts	1	0/3
Latch-Up VDD QJ1345	85 °C	JESD78	14.35 Volts	1	0/3
			5.80 Volts	1	0/3

Background Information:

Part #: CS3308 **Rev:** C0
Package: 48LQFP

Fab: MagnaChip (F)
Assembly: Siliconware (Taiwan)

Lead Finish: Pb-free

Prepared by: Rod Boutwell

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RELIABILITY QUALIFICATION REPORT

Report Date: 11/17/2008

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Reliability Report: QRR081106

<u>Stress</u>	<u>Conditions</u>	<u>Method</u>	<u>Duration</u>	<u>Lot</u>	<u>Results (Fail/sample)</u>
Latch-Up I/O QJ1345	85 °C	JESD78	+/-110 mA	1	0/3
Precondition MSL-3 QJ1426 (Similarity) QJ1427 (Similarity)	24HR 125 °C Bake 192HR 30°C/60%RH Soak 3 pass 260 °C Convection reflow	JESD22-A113	Precondition	1	0/231
			Precondition	2	0/231
HAST QJ1426 (Similarity)	130 °C 85 %RH 5.25 Volts	JESD22-A110	96 Hours	1	0/77
THB QJ1427 (Similarity)	85 °C 85 %RH 2.5 Volts 3.3 Volts	JESD22-A101	500 Hours 1000 Hours	1 1	0/77 0/77
Temperature Cycle cond. C QJ1426 (Similarity) QJ1427 (Similarity)	-65 °C +150 °C air to air	JESD22-A104	500 Cycles 500 Cycles	1 2	0/77 0/77
Tomography (CSAM) QJ1426 (Similarity) QJ1427 (Similarity)		J-STD-035	Post Temp Cycle 500 TCC	1 2	0/11 0/11
Autoclave/PPOT QJ1426 (Similarity) QJ1427 (Similarity)	121 °C 15 psig 100% R.H.	JESD22-A102	96 Hours 96 Hours	1 2	0/77 0/77
Solderability QJ1426 (Similarity) QJ1427 (Similarity)	93 °C steam aging 8 Hours 245 °C solder bath 5 Seconds	JESD22-B102	Solderability Solderability	1 2	0/15 0/15
HTSL (High Temp Storage Life) QJ1426 (Similarity) QJ1427 (Similarity)	150 °C	JESD22-A103	500 Hours 1000 Hours 500 Hours 1000 Hours	1 1 2 2	0/77 0/77 0/77 0/77

Background Information:

Part #: CS3308 Rev: C0
Package: 48LQFP

Fab: MagnaChip (F)
Assembly: Siliconware (Taiwan)

Lead Finish: Pb-free

Prepared by: Rod Boutwell

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DATE: 11-Oct-06

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IN HOUSE QUALIFICATION REPORT

CUSTOMER

SPIL

PACKAGE / PIN

LQFP 208(LF)/28*28*1.4

DEVICE

XXXXXXXX

APPROVED BY.

S.T. Liao
(QA dep. Manager)

CHECKED BY.

L.C. Chiang / Jack Lee
(Product Sec. Manager)

PREPARED BY.

Paul Lee
(PD engr.)

SPIL

Siliconware Precision Industries Co.,Ltd

RELIABILITY EVALUATION

PAGE : 2 OF 2

<u>ENVIRONMENT</u>	<u>READ POINT</u>	<u>SAMPLE SIZE</u>	<u>RESULT</u>
.SAT	ZERO HR	22	0/22
	PRE-CON LEVEL 3	22	0/22
. TEMPERATURE CYCLE (-65°C / 150°C)	1000 CYCLE	45	0/45
. PRESSURE COOKER (2ATM / 121°C)	168 HRS	45	0/45
. High Temp. Storage Life (150°C)	1000 HRS	45	0/45

SAMPLE PRECONDITIONING PRIOR TO ENVIRONMENTAL TESTS IS AS FOLLOW:

BAKING 125°C, 24 HRS --> PRE-CON :192 HRS 30°C / 60% RH --> IR 3X, 260°C

COMMENT

PASSED LEVEL-3 WITH IR260C TEST. PRODUCT CAN BE USED WITH IN 1 WEEK, AFTER REMOVAL FROM DRY-BACK.

SPIIL

Siliconware Precision Industries Co.,Ltd

Cirrus Logic PCN administrator: _____

Acknowledgement of Receipt of Notice:

Does customer waive PCN Effective Date? YES NO

Company Name: _____

Name (please print): _____ Title: _____

Signature: _____ Date: _____

Customer Representative is to obtain the customer acknowledgement/signature and return this notification to Cirrus Logic Corp. Quality, attn: PCN administrator at fax number (512) 851-4656

***NOTE: Lack of acknowledgement within 30 days of the date of notice, constitutes acceptance of change.
(Reference JEDEC Industry Standard: JESD-46)***